AMELIA LOBO

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EDUCATION

CARNEGIE MELLON UNIVERSITY Pittsburgh, PA

M.S. in Electrical & Computer Engineering (GPA: 4.0) May 2026

B.S. in Electrical & Computer Engineering (University Honors) May 2025

EXPERIENCE

ARM Austin, TX

Systems Validation Intern May 2025 - Aug. 2025

- Validation of Home Node (HN) on Coherent Mesh Network (CMN) product, stimulus generation, AMBA CHI architecture

ARM Austin, TX

RTL Design Intern May 2024 - Aug. 2024

- Implemented memory pooling feature on multi-chip link layer of CMN product in parameterized, synthesizable Verilog; passed all tests and merged into Arm upstream
- Designed packing logic for extended link-layer fields to support CXL protocol and internal channel communication (requests, responses, data, credits)

VOLVO GROUP Greensboro, NC

Driver Interaction & Connectivity Intern May 2023 - Aug. 2023

- Built Raspberry Pi app to parse CAN data and deliver real-time tractor-trailer warnings to Android tablet via Python app

PROJECTS

CUSTOM PCB & FPGA ENIGMA MACHINE CAPSTONE Jan. 2025 – May 2025

- Designed, synthesized RTL implementation of 3-rotor WWII-era Enigma machine on DE10-Standard FPGA, achieving 100% encryption accuracy
- Wrote and verified modular SystemVerilog FSMs for SPI, PS/2, and rotary encoder protocols to interface with custom PCB I/O peripherals, including lampboard, 7-segment displays, and rotary selector controls
- Received David Tuma Undergrad Project Runner-Up (49 teams total)

CUDA-OPTIMIZED CANNY EDGE DETECTION Jan. 2025 – May 2025

- Optimized 5×5 Gaussian blur in CUDA using shared memory tiling and thread-to-bank mapping on an NVIDIA T4 GPU
- Designed 4×5 per-thread tile layout, maximizing shared memory utilization under 48 KB and avoiding bank conflicts

RISC-V PROCESSOR CORE Jan. 2024 - May 2024

- Designed, verified, synthesized RISC-V processor core in SystemVerilog with full datapath, 5-stage pipeline, forwarding, stalling, branch prediction
- Improved branch prediction accuracy using 2-bit hysteresis counters and return address stack

USB PROTOCOL ENGINE Nov. 2023

- Designed, verified USB 2.0 serial interface engine in synthesizable SystemVerilog with NRZI encoding, bit-stuffing, CRC5/CRC16, ACK/NAK error handling, timeout counters

COURSEWORK

Modern Computer Architecture

Hardware Verification

How to Write Fast Code II (CUDA, OpenMP, SIMD)

Logic Design & Verification

SKILLS

HDLS

SystemVerilog, Verilog

PROGRAMMING LANG.

C/C++, Python, CUDA, OpenMP

PROTOCOLS

AMBA CHI, CXL

SIMULATION & SYNTHESIS

QuestaSim, Synopsys VCS, Quartus Prime

ARCHITECTURE & PERF

Gem5, McPAT, Cadence

ACTIVITIES

ECE PEER ADVISOR

Academic advising for ECE students, supporting schedule planning, course selection

STEM CAREER FAIR

Facilitated student and faculty communications for largest career fair at CMU, 80+ companies present

TEACHING ASSISTANT

Supported 150+ students in “Intro to ECE”, led office hours, graded homework

SWE, IEEE MEMBER

AWARDS & HONORS

College of Engineering Dean’s List: Spring 2022, Fall 2021, Fall 2024