# AMELIA LOBO

alobo@andrew.cmu.edu | (919) 670-8838 | https://amelia.lobo.codes/ | she/her

## EDUCATION

**CARNEGIE MELLON UNIVERSITY** — Pittsburgh, PA
B.S. in Electrical and Computer Engineering (GPA: 3.61) — May 2025
M.S. in Electrical and Computer Engineering — May 2026

## EXPERIENCE

**ARM** — Austin, TX
**RTL Design Intern** — May 2024 - Aug. 2024

- Implemented memory pooling feature on multi-chip link layer of coherent mesh network product in parameterized, synthesizable Verilog; passed all tests and merged into Arm upstream
- Designed new packing logic to support additional fields on link layer interface between CXL protocol and internal channels sending requests, responses, data, credits

**VOLVO GROUP** — Greensboro, NC
**Driver Interaction & Connectivity Intern** — May 2023 - Aug. 2023

- Developed RaspberryPi-based tractor-trailer integration app to provide driver with real-time data and warnings; received, parsed CAN messages and integrated formatted data with Android tablet python app

**CARNEGIE MELLON UNIVERSITY** — Pittsburgh, PA
**Teaching Assistant** | **ECE Department** — Jan. 2022 – May 2022

- Taught and reinforced course material for "Intro to Electrical and Computer Engineering" course comprised of 150+ undergraduate engineering students; held weekly office hours, graded homework and labs

## PROJECTS

**RISC-V PROCESSOR CORE** — Jan. 2024 - Apr. 2024

- Designed, verified, and synthesized RISC-V processor core in SystemVerilog
- Implemented full datapath, 5-stage pipelining, inter-stage forwarding and stalling logic, branch prediction
- Improved branch prediction accuracy using 2-bit hysteresis counters and return address stack

**USB PROTOCOL ENGINE** — Nov. 2023

- Designed and verified serial interface engine of USB 2.0 host in synthesizable SystemVerilog
- Implemented NRZI encoding, bit-stuffing, CRC5/CRC16 generation/checking, ACK/NAK generation, error processing, timeout counter hardware threads

**NETWORK ON CHIP** — Sep. 2023 - Oct 2023

- Designed and verified router-based packing switching network in parameterized synthesizable SystemVerilog
- Implemented nodes, routers, FIFO queue, and scheduling logic to handle and distribute pack loads across multi-router network
- Supports 32-bit packets being sent/received using ready/valid handshake

## COURSEWORK

Modern Computer Architecture (Fall '24)

Computer Architecture

Parallel Computer Architecture (Spring '25)

Logic Design & Verification

Hardware/Software Interface (Fall '24)

Computer Security

Computer Systems

## SKILLS

**HDLS**
SystemVerilog, Verilog

**SOFTWARE LANGUAGES**
C, C++, Python

**HDL SIMULATORS**
QuestaSim, Synopsys VCS, Quartus Prime

**TOOLS**
Gem5, McPAT, Cadence

**PROTOCOLS**
CXL

## AWARDS & HONORS

College of Engineering Dean's List: Spring 2022, Fall 2021

2020 FIRST Robotics Competition Dean's List Finalist

2020 NCWIT Award for Aspirations in Computing, Regional Award Winner

## ACTIVITIES

**SWE** | **STEM CAREER FAIR**
Facilitated student and faculty communications for STEM Career Fair (SCF), the largest career fair at Carnegie Mellon with 80+ companies present